EMI & Layout Checklist (Synchronous Buck)

[ ] Hot loop minimized (VIN -> HS FET -> SW -> CIN): MLCC close to FETs
[ ] Grounding: split AGND/PGND, single-point tie at IC pad; feedback routed away from SW
[ ] Inductor: shielded core; AC loss acceptable at chosen FSW and ripple
[ ] Sense point: remote sense at load (if available) or at Cout pad
[ ] Gate drive: loop area minimized; check dv/dt shoot-through; dead-time verified
[ ] Snubbers/RC damping implemented as needed; check ringing on SW node
[ ] Input filter: check interaction with control loop (avoid peaking/instability)
[ ] Probing: short ground spring, coax for SW; LISN for conducted; near-field scan if available
[ ] Compliance pre-check: CISPR 22/32 (IT), CISPR 25 (auto), IEC61000-4-X as applicable